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(54) **METHOD AND SYSTEM FOR MODIFYING SUBSTRATE RELIEF FEATURES USING ION IMPLANTION**

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(57) **ABSTRACT**

A method of treating resist features comprises positioning, in a process chamber, a substrate having a set of patterned resist features on a first side of the substrate and generating a plasma in the process chamber having a plasma sheath adjacent to the first side of the substrate. The method may further comprise modifying a shape of a boundary between the plasma and the plasma sheath with a plasma sheath modifier so that a portion of the shape of the boundary is not parallel to a plane defined by a front surface of the substrate facing the plasma, wherein ions from the plasma impinge on the patterned resist features over a wide angular range during a first exposure.

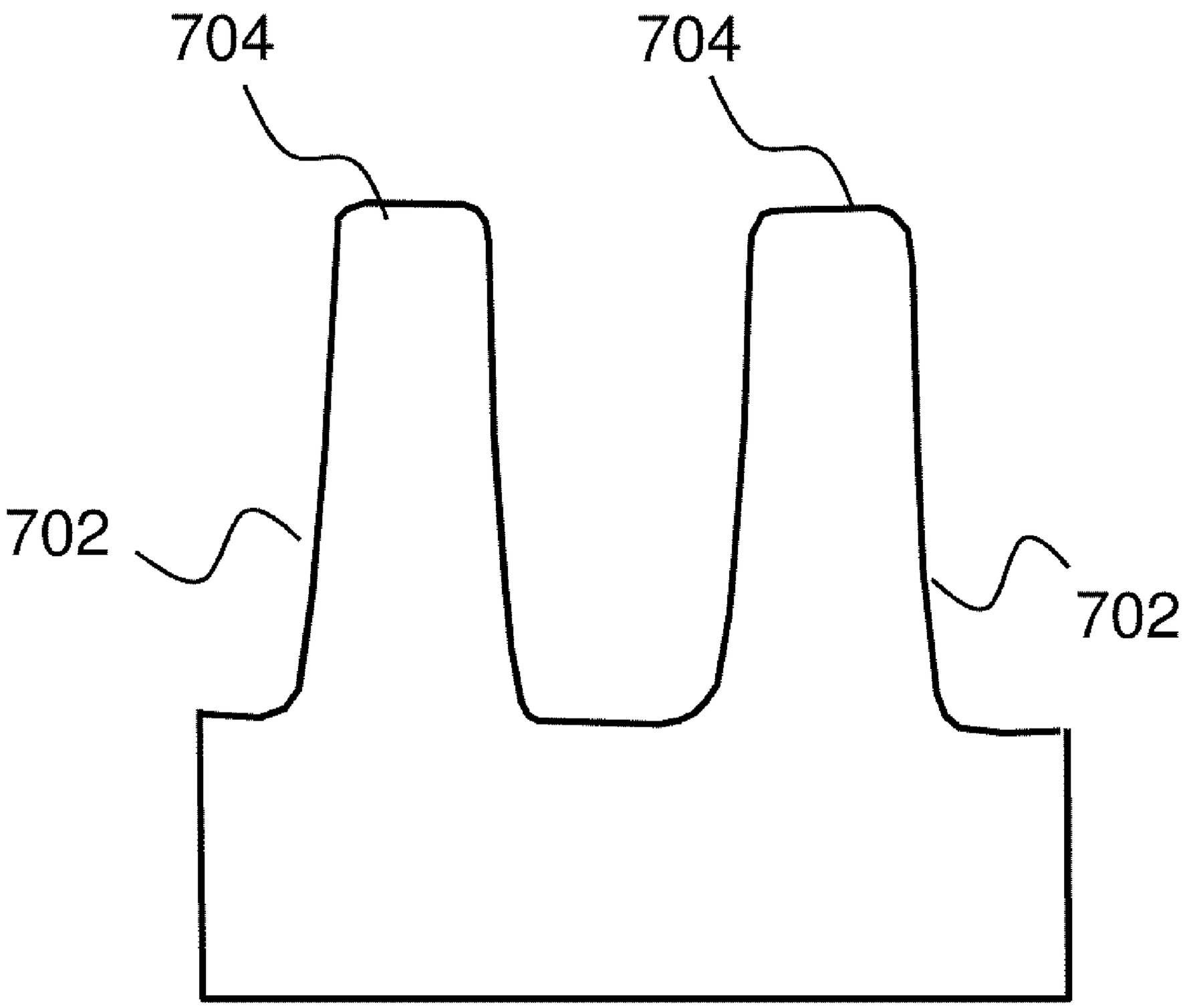



FIG. 1c

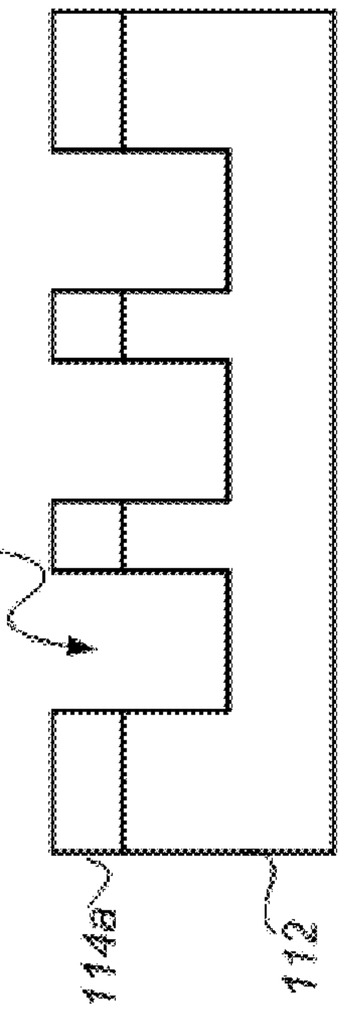

FIG. 1d

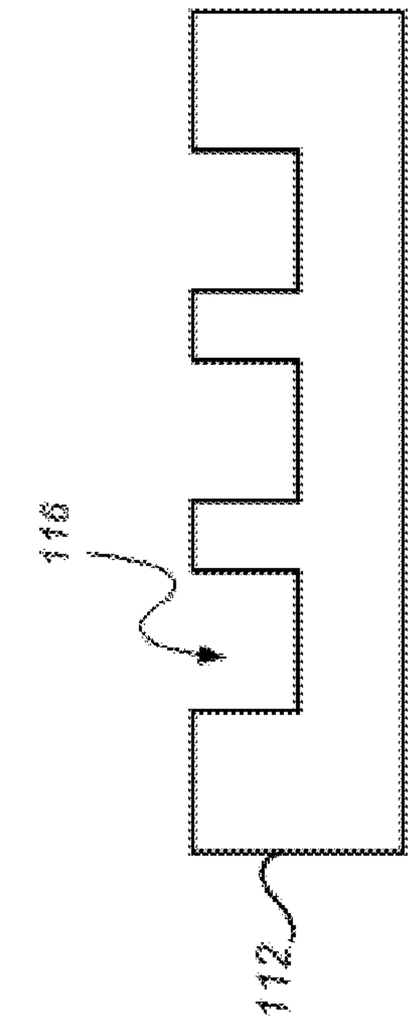

FIG. 1e

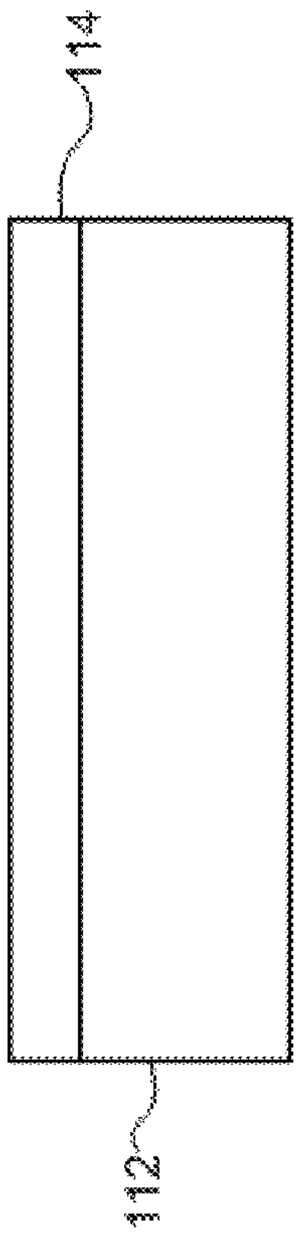

FIG. 1a

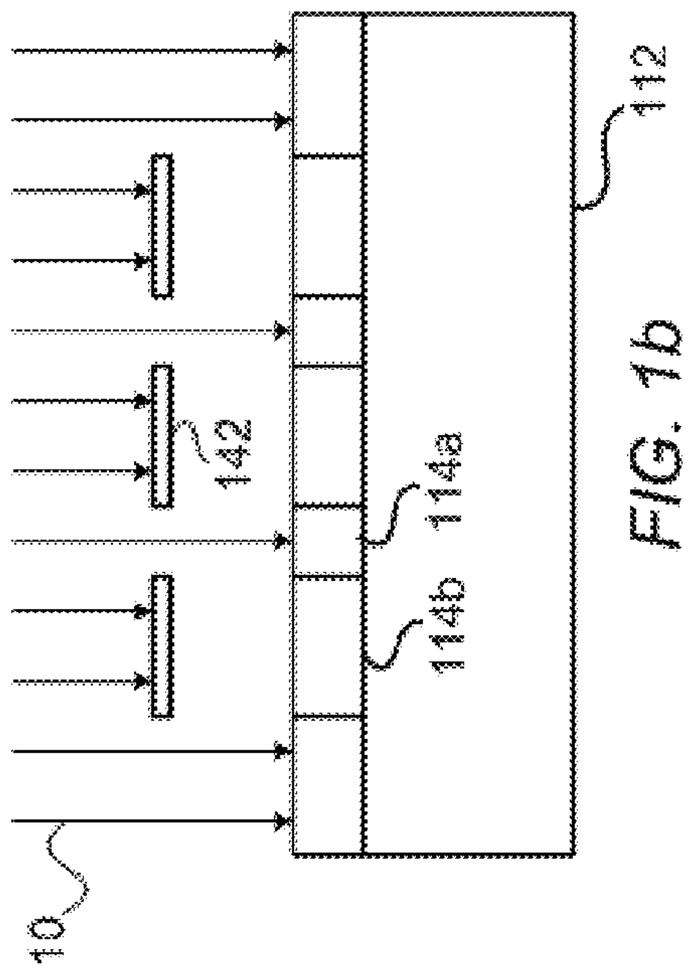

FIG. 1b

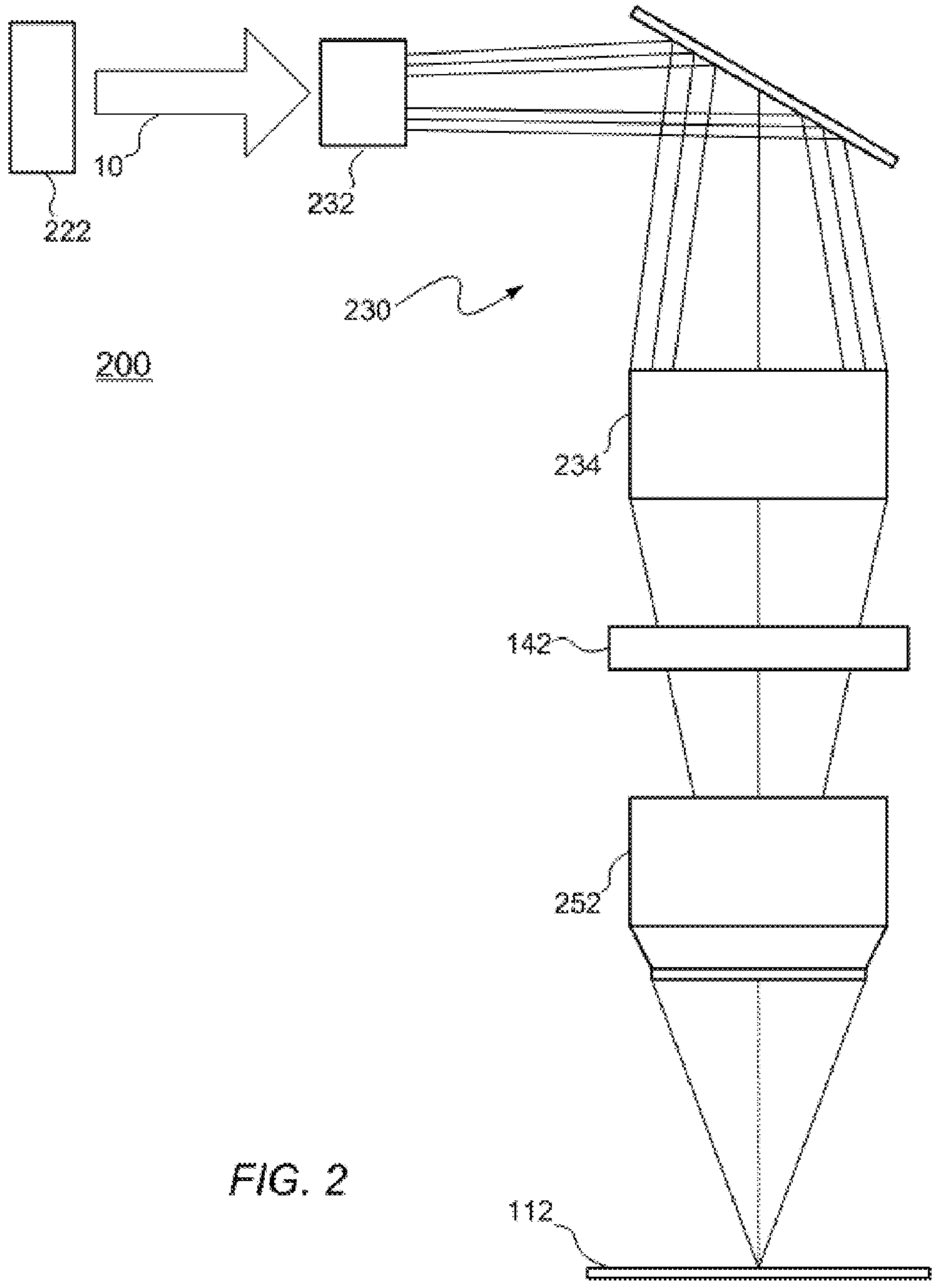

FIG. 2

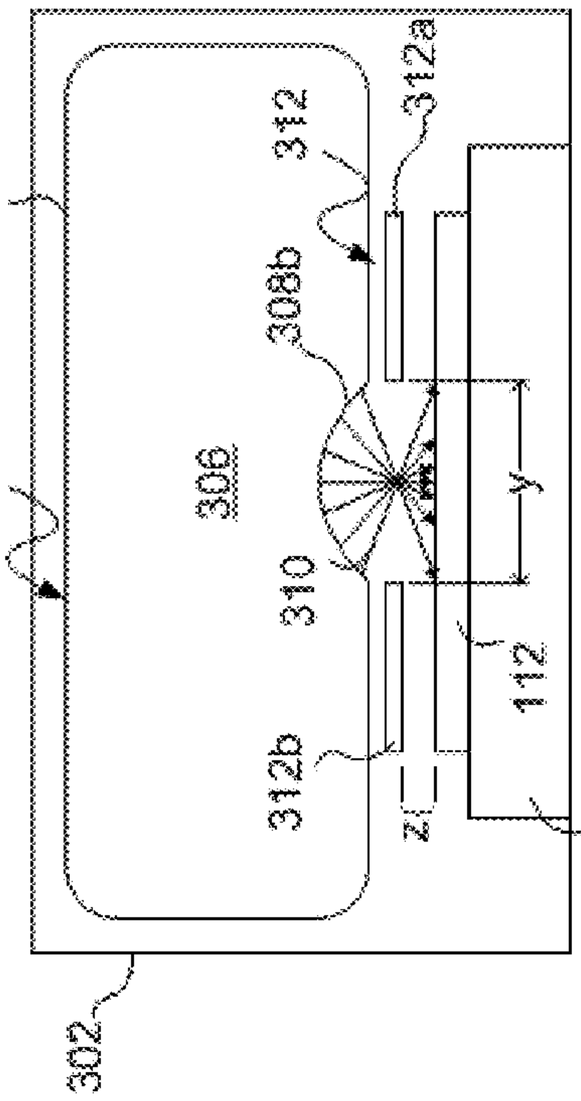

FIG. 3a

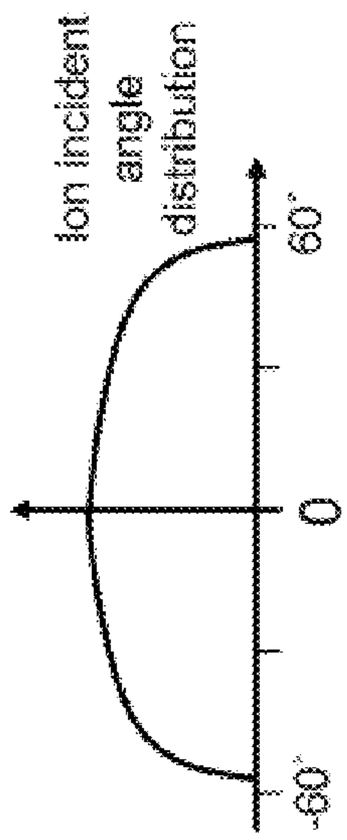

FIG. 3b

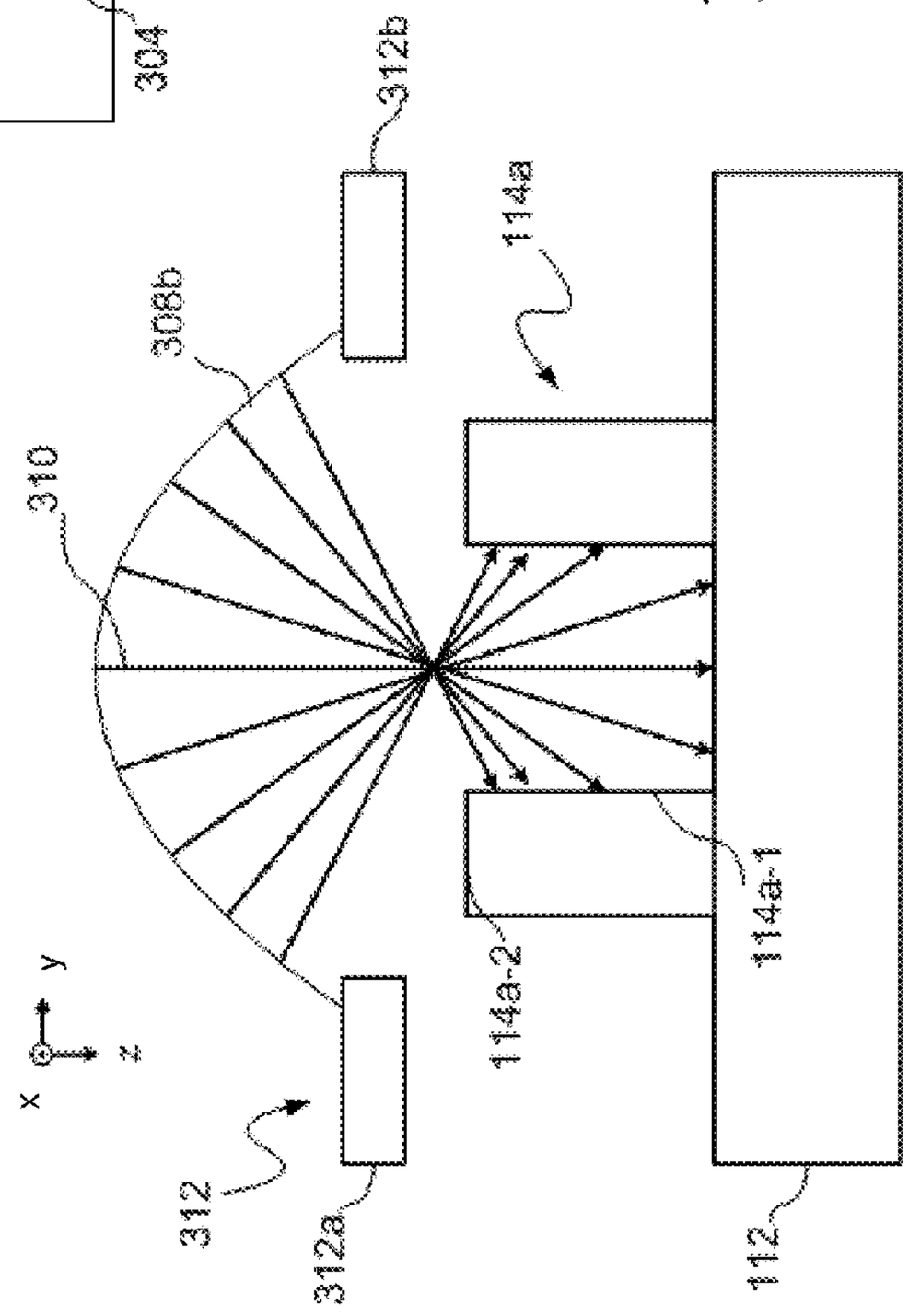

FIG. 4

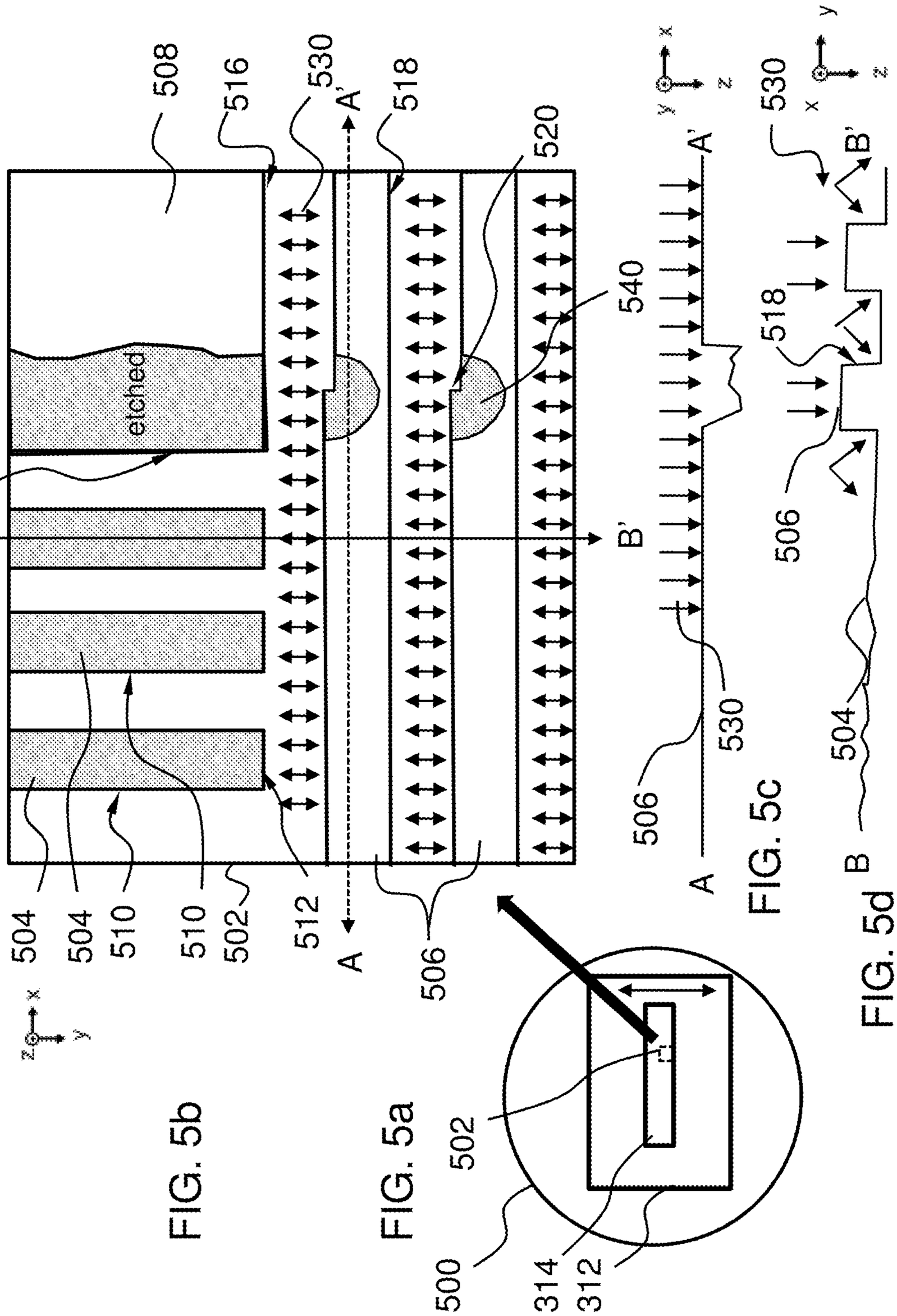

FIG. 5b

FIG. 5a

FIG. 5c

FIG. 5d

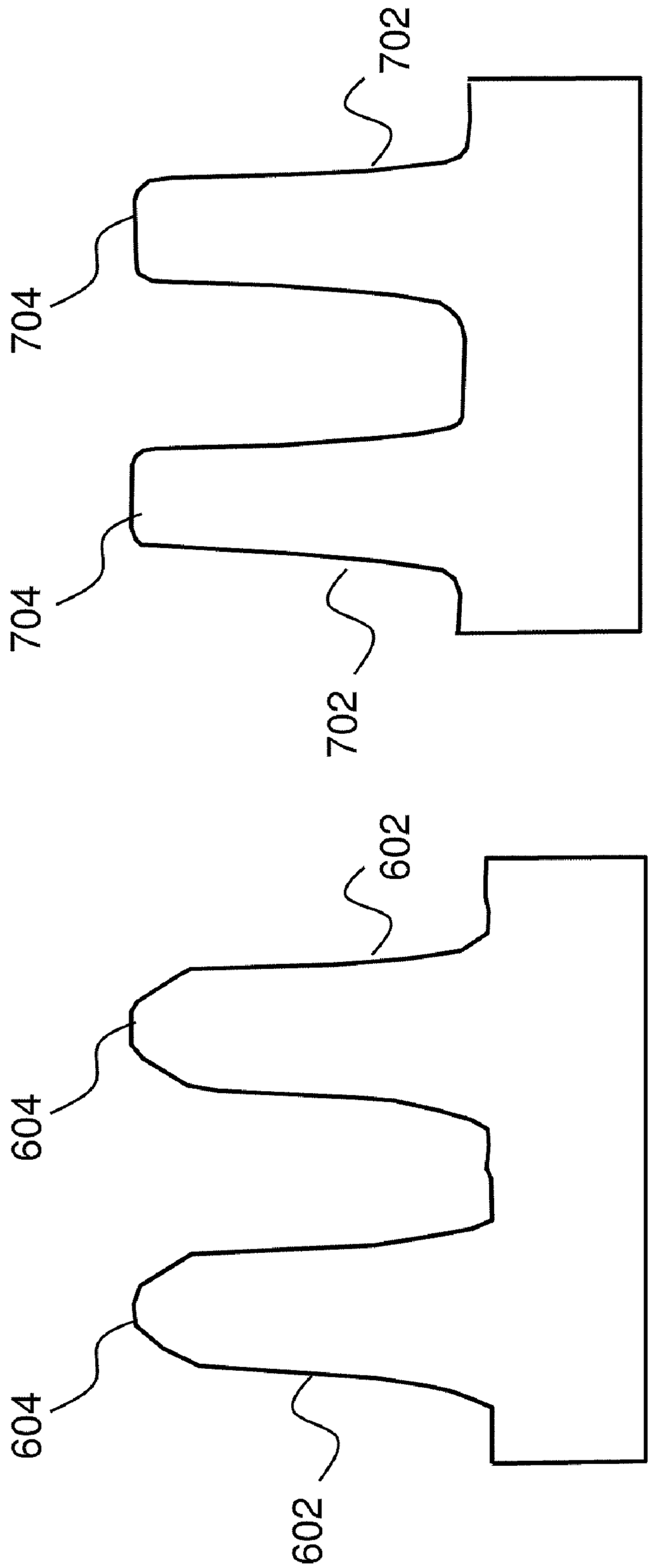

FIG. 7

FIG. 6

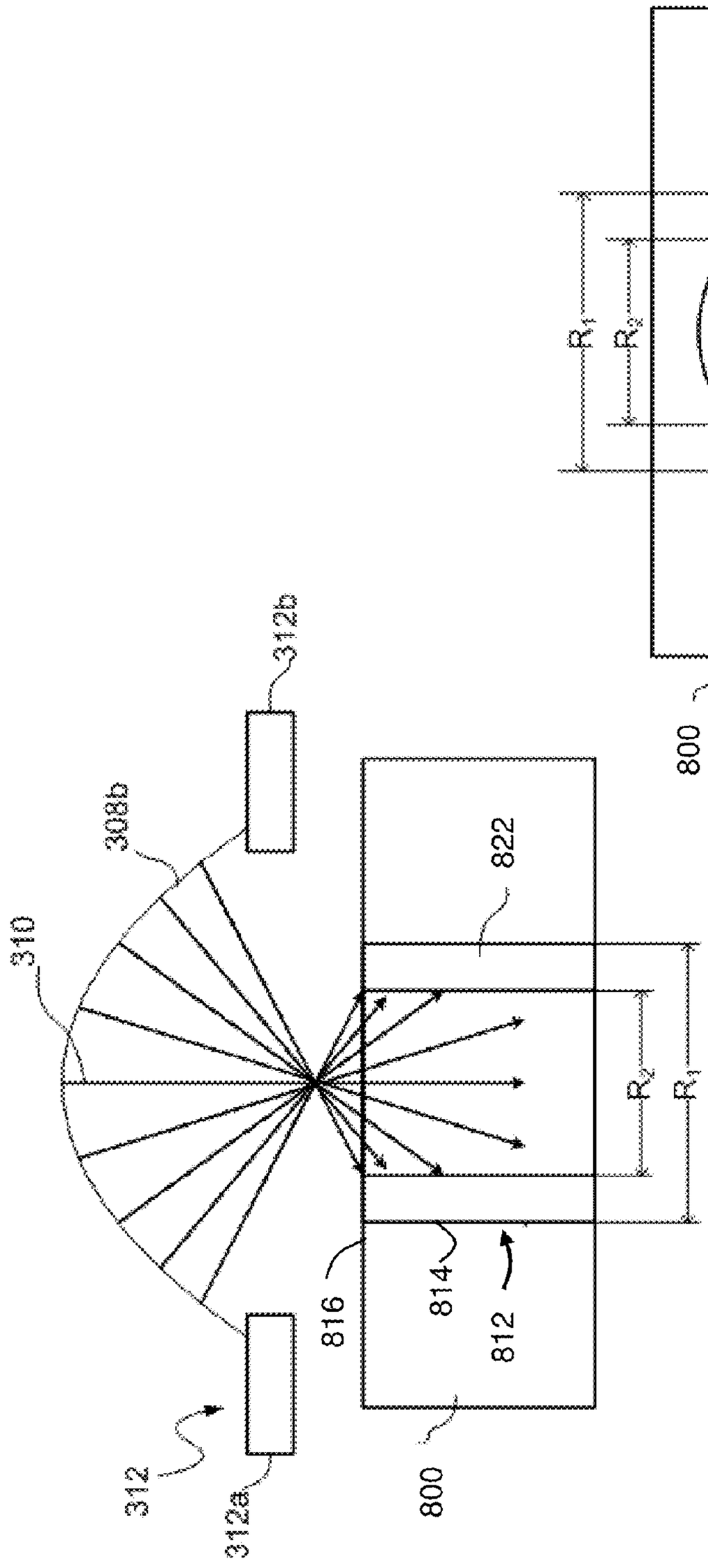
310
308b
312b
822
R_2
R_1
816
814
812
800
312
312a

FIG. 8a

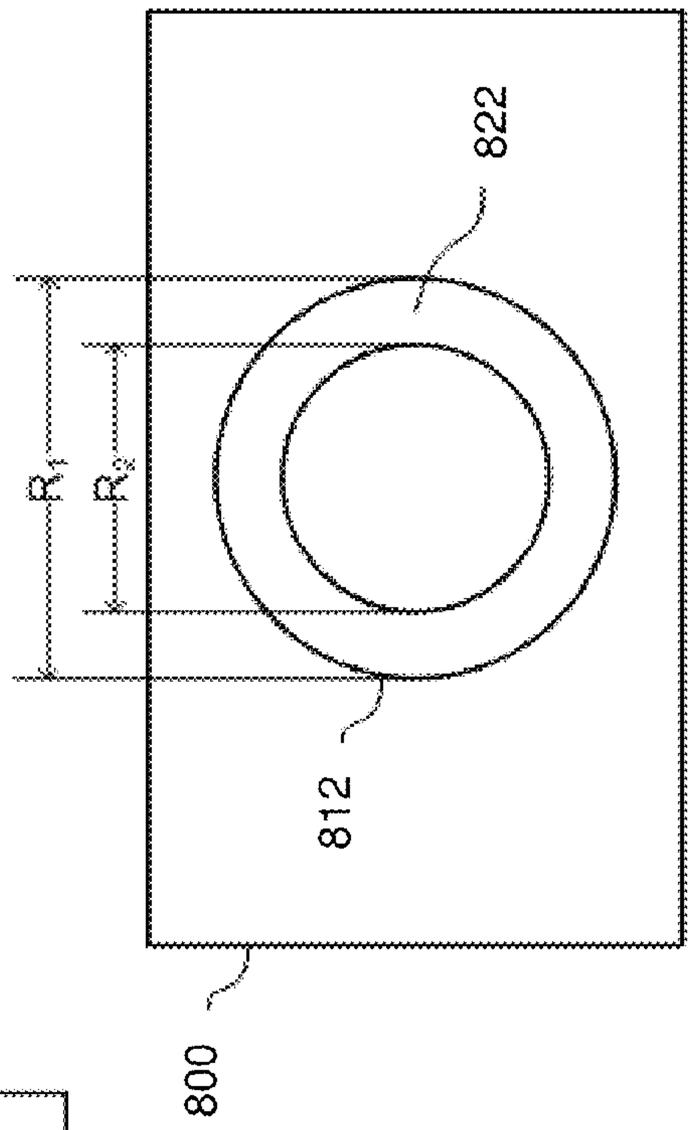
822
R_1
R_2
812
800

FIG. 8b

METHOD AND SYSTEM FOR MODIFYING SUBSTRATE RELIEF FEATURES USING ION IMPLANTION

[0001] This application claims priority to U.S. provisional patent application serial number 61/340,268, filed Mar. 15, 2010, and incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] Embodiments of the invention relate to the field of device manufacturing. More particularly, the present invention relates to a method, system and structure for patterning a substrate and for implanting into a substrate for manufacturing a device.

[0004] 2. Discussion of Related Art

[0005] Optical lithography is often used in manufacturing electronic devices. It is a process by which a substrate is patterned so that circuit may be formed on the substrate according to the pattern. Referring to FIG. **1***a*-**1***e*, there are shown simplified illustrations of the optical lithographic process. Generally, the substrate **112** is coated with photo-curable, polymeric photoresist **114** (FIG. **1***a*). Thereafter, a mask **142** having a desired aperture pattern is disposed between the substrate **114** and a light source (not shown). The light **10** from the light source is illuminated onto the substrate **112** via the aperture of the mask **142**, and the light transmitted through the mask's aperture (or the image of the pattern) is projected onto the photoresist **114**. A portion of the photoresist **114***a* is exposed to the light **10** and cured, whereas the rest of the photoresist **114***b* remains uncured (FIG. **1***b*). As a result, an image of the mask's apertures may form by the cured portion of the photoresist **114***a*.

[0006] As illustrated in FIG. **1***c*, the uncured portion of the photoresist **114***b* is stripped, and 3D photoresist feature or relief **114***a* corresponding to the mask's aperture pattern may remain on the substrate **112**. Thereafter, the substrate is etched, and trenches **116** corresponding to the negative image of the mask's aperture pattern may form (FIG. **1***d*). After the remaining photoresist **114***b* is removed, a patterned substrate **112** may form (FIG. **1***e*). If a metallic layer is deposited on the trenches, a circuit having a desired pattern may be formed on the substrate **112**.

[0007] Referring to FIG. **2**, there is shown a conventional optical lithographic system **200** for projecting the image of the mask's aperture pattern to the substrate. The optical lithography system **200** comprises a light source **222**, an optical integrator **232**, and a condenser lens **236**. In addition, the optical lithography system **200** may comprise mask **142** having a desired aperture pattern and a projection lens **252**. As illustrated in the figure, light having desired wavelength is emitted from the light source **222** to the optical integrator **232** and the condenser lens **234**, which are collectively known as an illuminator **230**. In the illuminator **230**, the light **10** is expanded, homogenized, condensed, or otherwise conditioned. The light **10** is then illuminated onto the mask **142** having the desired aperture pattern to be projected onto the substrate **112**. The light **10** transmitted through the apertures of the mask **142** may contain the information on the mask's aperture pattern. The light **10** is then captured by the projection lens **252** which projects the light **10** or the image of the mask's aperture pattern onto the photoresist deposited on the substrate **112**. In projecting the image, the projection lens **10** may reduce the image by a factor of four or five.

[0008] To generate circuit patterns with smaller feature size (e.g. width of the trench), several modifications have been implemented into the process. As known in the art, the ability to project a clear image of a small feature may depend on, among others, the wavelength of the light used in the process. Currently, UV light with wavelengths of 365 nm and 248 nm, and 193 nm are used. In particular, to generate circuits with 13.5 nm width, argon fluoride (ArF) excimer laser with 193 nm have been proposed.

[0009] Although optical lithography is an efficient process with high throughput, the process is not without disadvantages. One disadvantage may include line width roughness (LWR) or line edge roughness (LER). As known in the art, LWR is excessive variations in the width of the photoresist feature formed after uncured portion of the photoresist **114***b* is stripped from the substrate. If the variations occur on the side surface of the photoresist relief or feature, the variations is known as LER. The roughness or variations due to LWR or LER may be disadvantageous as the variation may be transferred onto the trenches during etch and ultimately to the circuit. The variations become more significant with decrease in feature size of the photoresist relief or trenches. For example, variations of 4 nm or larger have been observed a 193 nm based lithographic process producing 13.5 nm feature size. Because the geometrical shape of a patterned resist feature, including line roughness effects, such as LWR and LER, is transferred from a resist layer to an underlying permanent layer of a device during patterning of the underlying layer, LWR and LER can limit the ability to form devices of acceptable quality for dimensions below about 100 nm. Such variations may lead to non-uniform circuits and ultimately device degradation or failure. In addition, depending on design criteria, device performance may be impacted more by either one of short, medium, or long range roughness.

[0010] Several approaches have been attempted to address LWR and LER effects. In one example, dry chemical etch process has been employed which has the ability to remove resist, but generally suffer from pattern dependent loading effects in which the removal is different in densely patterned regions as opposed to isolated features. Such dry chemical etching processes may also impart unwanted defects into a resist pattern, which could result in yield loss. In addition, it is important that any process used to address LWR/LER effects in resist, leave the original resist attributes, such as resist height, width, and profile, intact, in order to maintain tight control of the critical dimension (CD) of underlying features to be patterned.

[0011] Another approach used to address LWR and LER effects has been to use deep ultraviolet (DUV) curing by exposing a rough pattern to a UV lamp in which heating through radiation exposure is used to smooth out rough lines. This approach has the unwanted side effect of causing pattern pullback at line segment corners, causing lines to deform in such a way as to render devices useless.

[0012] In order to address the diffraction limit of UV lithography processing of resist, where lines or other patterns may have CD feature sizes below the diffraction limit of the illuminating radiation, double patterning lithography (DPL) has been developed. Multiple approaches have been employed in an attempt to ensure success of DPL, including self aligned double patterning lithography and chemical freeze lithography.

[0013] However, each of these processes may have both advantages and disadvantages with respect to cost and/or yield.

[0014] In addition to the aforementioned challenges regarding control of resist patterning, control of the size and shape of patterned substrate features after their formation remains a challenge. It is well known that controlling the etching conditions for patterning substrate features used to form devices, such as polysilicon or metal gates, or silicon fins, may be critical in defining the eventual shape and size of such features after etching. In addition, processing steps such as ion implantation may affect the shape and size of such substrate features, especially those having dimensions on the order of 100 nm or less. For example, ion implantation of substrates to provide doping of devices having silicon fins may inadvertently cause etching/sputtering of the fins. In some cases, the silicon fins may develop pronounced faceting, which may substantially alter device properties of fin-based devices to be formed.

[0015] In view of the above, it will be appreciated that there is a need to improve processes that affect device feature patterning, such as resist lithography processes and device doping processes, especially for technologies requiring very small feature sizes, such as sub-100 nm CD devices.

SUMMARY OF THE INVENTION

[0016] Embodiments of the present invention are related to methods and systems for improving patterning a substrate, in particular, by treating relief features such as patterned resist features or permanent patterned substrate features. In one example, a method of treating resist features comprises positioning, in a process chamber, a substrate having a set of patterned resist features on a first side of the substrate and generating a plasma in the process chamber having a plasma sheath adjacent to the first side of the substrate. The method may further comprise modifying a shape of a boundary between the plasma and the plasma sheath with a plasma sheath modifier so that a portion of the shape of the boundary is not parallel to a plane defined by a front surface of the substrate facing the plasma, wherein ions from the plasma impinge on the patterned resist features over a wide angular range during a first exposure.

[0017] In another embodiment, a method of patterning a substrate, comprises providing a first set of patterned resist features on the substrate. The method further comprises exposing the first set of patterned resist features to a first exposure of ions extracted from a plasma sheath modifier operable to provide ions incident on the substrate over a wide angular range and performing a lithographic patterning process on the substrate to form a second set of patterned resist features.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIGS. **1***a*-**1***e* are schematic cross-sections of a substrate that illustrate steps of a conventional optical lithographic process.

[0019] FIG. **2** is a schematic depiction of a conventional optical lithographic system for projecting the image of a mask's aperture pattern onto a substrate.

[0020] FIG. **3***a* is a schematic depiction of a substrate processing system, in accordance with one embodiment of the present invention.

[0021] FIG. **3***b* illustrates an exemplary angular distribution of incident particles on a substrate, as provided by embodiments of the present invention.

[0022] FIG. **4** depicts a schematic cross section of a plasma sheath modifier and a resist feature that illustrate exemplary features of the invention.

[0023] FIGS. **5***a*-**5***d* depict exemplary results of an embodiment of processing a 3D resist pattern.

[0024] FIG. **6** depicts patterned silicon features after exposure to known ion implantation.

[0025] FIG. **7** depicts patterned silicon features after exposure to an exemplary wide angular range of ion flux.

[0026] FIG. **8** depicts an embodiment of 3D processing.

DESCRIPTION OF EMBODIMENTS

[0027] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention, however, may be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, like numbers refer to like elements throughout.

[0028] To solve the deficiencies associated with the methods noted above, novel and inventive techniques and systems for patterning a substrate are introduced. In some embodiments, methods may involve treating temporary substrate features that are to be eventually removed, such as patterned photoresist features. In other embodiments, methods may involve treating permanent device features, such as semiconductor structures. In particular, the present disclosure focuses on techniques involving ion implantation processes for improving the quality of resist features, such as improving LWR and LER in resist features. The processes disclosed herein may be used in conjunction with processes for forming narrow features, including features that are incorporated into arrays having very small pitch, for example a pitch less than about 250 nm. Such processes include conventional DUV lithography, double patterning lithography, self aligned double patterning lithography, and other lithographic processes. However, those of ordinary skill in the art will recognize that the techniques disclosed herein are not limited to use in conjunction with any particular lithography or any range of resist feature dimensions.

[0029] Some embodiments of the invention employ plasma immersion implantation processes to treat resist features having very small dimensions. Several embodiments comprising new techniques for processing three dimensional (3D) structures are disclosed. For the purposes of clarity and simplicity, the embodiments are described as techniques for processing photoresist having surfaces oriented at multiple angles. However, those of ordinary skill in the art will recognize that the present disclosure is not limited thereto. The structure may be any type of structure having surfaces oriented at different angles.

[0030] The embodiments are also described as techniques using plasma based substrate processing systems. However, those of ordinary skill in the art will recognize that other types of sub-atomic, atomic, or molecular particle based substrate processing systems, including plasma sputtering, as well as beam line ion implantation systems, are within the scope of the present disclosure

[0031] Referring to FIG. **3***a*, there is shown a substrate processing system **300** for processing a 3D structure according to one embodiment of the present invention. FIG. **3***b* illustrates angular distribution of the particles treating the photoresist. The figures are not necessarily drawn to scale.

[0032] As illustrated in FIG. **3***a*, the system **300** may include a process chamber **302** in which the substrate **112** and a platen **304** supporting the substrate **112** are disposed. In the present disclosure, the substrate **112** may be a metallic, semiconducting, or insulating material based substrate. In the present disclosure, patterned photoresist may be disposed on the substrate. The patterned photoresist may be a cured portion of the photoresist remaining on the substrate after the uncured portion is stripped.

[0033] The system **300** may also include a plasma source (not shown) for generating plasma **306** contained in the processing chamber **302**. The plasma source may be an in situ or remote, inductively coupled plasma source, capacitively coupled plasma source, helicon source, microwave source, or any other type of plasma source.

[0034] Between the plasma **306** and the substrate **112**, one or more plasma sheath modifiers **312** may be disposed. In the present embodiment, the plasma sheath modifier **312** may comprise a pair of modifier parts **312***a* and **312***b* spaced apart from one another by a gap "y." In another embodiment, the modifier **312** may comprise a single modifier part. Yet in other embodiments, the modifier **312** may comprise three or more modifier parts spaced apart from one another defining the gap.

[0035] The plasma sheath modifier **312** is capable of adjusting the electric field of the plasma sheath. In some embodiments, the plasma sheath modifier **312** may be positively or negatively charged. The plasma sheath modifier **312** may be made from electrically insulating (e.g. glass) or conducting (e.g. metallic) material, or a combination thereof. If the system **300** includes more than one modifier parts, the parts may be made from the same or different material. For example, the system **300** may include a plasma sheath modifier **312**, and the plasma sheath modifier **312** may comprise two modifier parts **312***a* and **312***b*. The modifier parts **312***a* and **312***b* may be made from the same or different material.

[0036] If the plasma sheath modifier **312** comprises two or more parts, the parts may be disposed on the same plane or different planes. For example, the plasma sheath modifier **312** included in the processing system **300** may comprise two modifier parts **312***a* and **312***b*. The parts **312***a* and **312***b* may be disposed in the same plane such that the vertical spacings "z" between the substrate **112** and each modifier part are the same. In another embodiment, the modifier **312** may comprise two modifier parts **312***a* and **312***b*, and each part **312***a* and **312***b* may be spaced apart from the substrate **112** by different vertical spacings Additional description of the processing system with the plasma sheath modifier can be found in co-pending U.S. patent application Ser. Nos.: 12/418,120; 12/417929, filed Apr. 3, 2009, and issued as U.S. Pat. No. 7,767,977; and 12/644103, each of which is herein incorporated in its entirety by reference.

[0037] In operation, plasma generated in situ or remotely may be contained in the processing chamber **302**. The plasma **306** may contain fragments including electrons, proton, and atomic or molecular ions, neutrals, and radicals of desired species. In the present disclosure, the plasma fragments **306** may be used to dope, etch, or deposit material on the substrate **112**. The species contained in the plasma **306** are not limited to one or more particular species. The species may include one or more elements from Group I and **3**A-**8**A. Example of the species contained in the may include hydrogen (H), helium (He) or other rare gases, carbon (C), oxygen (**0**), nitrogen (N), arsenic (As), boron (B), phosphorus (P), antimony, gallium (Ga), indium (In), carborane $C_2B_{10}H_{12}$ or other molecular compounds. As illustrated in FIG. **3**, the plasma **306** may also include plasma sheath **308** near the periphery. In the present embodiment, the plasma sheath **308** may comprise positively charged ions **310**.

[0038] As depicted in the Figures, sheath **308** is represented by a boundary of the sheath with plasma **306**. However, it will be understood that sheath **308** may extend a finite distance from an edge of plasma **306** to surfaces of objects around plasma **306**, for example, the walls of chamber **302**, and the surface of substrate **112**.

[0039] The ions **310** in the plasma sheath **308** or the plasma **306** may be directed toward the substrate **112**, as the substrate **112** is biased by a DC or RF bias supply (not shown). The bias signal applied to the substrate **112**, whether DC or RF, may be continuous or pulsed.

[0040] The plasma sheath modifier **312** may modify the shape of the plasma sheath **308** so as to control the incident angle distribution of the ions **310**. For example, the plasma sheath modifier **312** may modify the electric field in the plasma sheath **242** and modify the shape of the plasma sheath **308**. In the present embodiment, the plasma sheath modifier **312** may modify at least a portion of the sheath **308** into a concave shaped plasma sheath **308***b* (modified sheath **308***b*) relative to the bulk plasma **306**, or a dome shaped (convex) plasma relative to the bulk plasma. When the substrate **112** is biased, the ions **310** attracted toward the substrate **112** may travel through the gap "y" between the modifier parts **312***a* and **312***b* at a large range of incident angles. In the conventional plasma based processing systems, the plasma sheath closest to the substrate lies parallel to the substrate. When the substrate is biased, the ions travel in a path substantially perpendicular to the plasma sheath, thus substantially perpendicular to the substrate. As a result, the ions in the conventional plasma processing system have incident angle ranging from −3° −+3°. In the present embodiment, however, the incident angle of the ions **310** may be modified with the modified sheath **308***b*. As illustrated in FIG. **3***a*, the modified sheath **308***b* is multi-angled relative to the substrate. As such, ions **310** traveling perpendicular to the modified sheath **308***b* may travel in multiple angles. The ions **310** traveling toward the substrate **112** from different portions of the modified sheath **308***b* may have different incident angles, and the ions **310** will therefore have a large range of incident angles. As illustrated in FIG. **3***b*, the incident angles of the ions **310** may range between about +60° to about −60° , centered about 0°. In some embodiments, the incident angles of the ions **310** may additionally be modified by the electric field generated by the plasma sheath modifier **312**.

[0041] Depending on a number of factors including, but not limited to, configurations and properties of the plasma sheath modifier **312**, the incident angle of the ions may be additionally modified. Example of such factors may include the horizontal spacing (Y) between the modifier parts **312***a* and **312***b*, the vertical spacing (Z) between the modifier **312** and the substrate **112**, difference in the vertical spacing (z) between the substrate **112** and each modifier parts **312***a* and **312***b* (not shown), and the electrical properties of the modifier **312**. Other plasma process parameters may also be adjusted to adjust the ions' incident angle and/or incident angle distribu-

tion. Additional description may be found in the co-pending U.S. patent application Ser. No.: 12/418,120, 12/417929, 12/644103, each of which application, as noted above, is incorporated in entirety by reference.

[0042] By modifying the plasma sheath **312**, a three dimensional structure with surfaces oriented at different angles may be treated conformally or isotropically. As noted below, the modified plasma sheath **312** may be used to treat multiple surfaces of 3d structures such as, for example, 3D photoresist reliefs isotropically at the same time.

[0043] Referring to FIG. **4**, there is shown a technique for processing 3D structure according to one embodiment of the present invention. In the present embodiment, the technique may be used to reduce LER and LWR contained in 3D photoresist relief **114***a*. As noted above, LER and LWR may occur in 3D photoresist relief **114***a* obtained during optical lithography, after uncured portion of the photoresist resist is removed. In the present embodiment, LER and LWR contained in the photoresist relief **114***a* may be reduced by performing plasma assisted doping (PLAD) or a plasma immersion ion implantation (PIII) process using the plasma sheath modifier **312** on different surfaces of the relief **114***a*. Those of ordinary skill in the art will recognize that the figure is not necessarily drawn to scale.

[0044] As illustrated in FIG. **4**, 3D photoresist relief **114***a* having side surface **114***a*-**1** and top surface **114***a*-**2** may be disposed on the substrate **112**. The substrate **112** and the photoresist relief **114***a* disposed in the plasma processing system containing the plasma sheath modifier **312**, and plasma is disposed near the substrate **112**. Thereafter, the ions **310** in the plasma may be directed through the gap between the plasma sheath modifier parts **312***a* and **312***b*, toward the surfaces of the photoresist relief **114***a*. As illustrated in the figure, the ions **310** may be directed at multiple incident angles.

[0045] In the present embodiment, the ions **310** may be implanted into the side and top surfaces **114***a*-**1** and **114***a*-**2** of the photoresist relief **114***a*. Although various ion species may be implanted, helium (He) or argon (Ar) ions may be implanted in the present invention. Although the duration of exposure of the resist to ions may cover a wide range, in embodiments of the present invention, the exposure time may vary from about one second to several minutes.

[0046] Experiments were conducted to study the effect on LER of a plasma processing system (PSM system) arranged in accordance with the present invention. As used hereinafter, the term "PSM system" or "PSM plasma system" refers to a plasma processing system that employs a plasma sheath modifier to provide a wide range of angular distribution of ions toward a substrate positioned adjacent to a portion of the plasma. The term "wide," "wide range," or "wide angular range," as used in conjunction with angle of ion incidence, refers to a set of angles that spans a total range of about 5 degrees or larger. A plasma sheath modifier was used to provide an exposure comprising a dose of ions distributed over a wide angular range, as illustrated in FIG. **3***b*. In some instances, the term "extraction plate" may be used to refer to a plasma sheath modifier, which may comprise a plate having an aperture that induces formation of a modified plasma sheath (see element **308***b*) and also extracts ions from the plasma such that the ions impinge on a substrate over a wide angular range.

[0047] Referring again to FIG. **4**, a set of resist lines having nominal CD of about 40 nm was exposed to a 3 kV He plasma using an exemplary extraction plate. By implanting He ions **310** into both the top **114-2** and side **114***a*-**1** surfaces of the photoresist relief **114***a* at 3-4 kV, the LER improved from 5.6 to 3.2 nm, and an improvement of about 40% in LER and LWR was observed. By implanting He ions using the plasma sheath modifier **312**, the improvements occurred isotropically, on the multiple surfaces **114***a*-**1** and **114***a*-**2** of the photoresist relief **114***a*, at the same time.

[0048] In addition, only minimal critical dimension shrinkage of the photoresist relief **114***a* was observed. In particular, the measured CD before processing of 39.1 nm was only reduced to 37.6 nm after processing, representing only a 4% shrinkage when the resist relief **114***a* was implanted with He ions **310** at multiple incident angles. Minimal faceting or sputtering was also observed. As PLAD or PIII process is a low energy process, the depth by which the ions **310** are implanted is very low. As such, any change to the photoresist relief **114***a* caused by ion implantation such as, for example, resist shrinkage and/or sputtering may be minimal.

[0049] In various embodiments, an optimum line roughness for patterned resist features may depend upon the nature of the devices to be fabricated in an underlying substrate using the patterned resist. Accordingly, in embodiments of the present invention, a set of parameters may be tuned to produce an optimum reduction in desired roughness features. These parameters may include, among others, ion type, ion energy, resist type, resist feature size, as well as geometrical features associated with the plasma sheath modifier. With reference again to FIG. **3***a*, the latter features include the horizontal spacing Y, vertical spacing Z, and other factors, which are disclosed in more detail in the co-pending U.S. patent application Ser. Nos.: 12/418,120, 12/417929, and 12/644103 .

[0050] The aforementioned exemplary systems, methods, and compositions may, in general, be used in any combination to provide improved roughness results, such as reductions in LWR/LER, reductions in high, low, and medium frequency roughness variations, and similar patterned resist attributes.

[0051] In addition to reducing linewidth roughness, concurrent, isotropic hardening of multiple surfaces of photoresist features may be induced according to some embodiments. Referring again to FIG. **4**, after exposure to wide angular range of ion flux, isotropic hardening has been observed in patterned resist features generally depicted as photoresist relief **114***a*. Concurrent, isotropic hardening of the photoresist relief **114***a* may be advantageous if an additional optical lithographic process is performed to achieve double patterning lithographic (DPL) or self-aligned double patterning lithographic (SADPL) process. In DPL or SADPL, a second lithographic process is performed to generate additional photoresist reliefs between two original photoresist reliefs formed during the first lithographic process. Forming additional photoresist reliefs may decrease the distance therebetween and may lead to a substrate **112** with trenches with even smaller widths. During the second lithographic process, a chemical treatment may be performed. When performed, the structure of the photoresist relief formed during the first lithographic process may be adversely affected. In the present embodiment, isotropically hardened photoresist relief **114***a* may be able to withstand the chemical treatment associated with the second lithographic process. As such, an additional lithographic process to achieve DPL or SADPL may be possible.

[0052] FIGS. **5***a*-**5***d* depict exemplary results of an embodiment of processing a 3D resist pattern. In this example, several different types of resist features were subjected to an ion exposure using an exemplary extraction plate (plasma sheath modifier) to provide a wide angular range of ions in order to clarify the operation of exemplary resist hardening processes. Referring to FIG. **5***a*, a substrate **500** includes a portion **502** that is subjected to an exemplary exposure to a wide angular distribution of ions using an exemplary plasma sheath modifier, such as plate **312**. In the example of FIG. **5***a*, a plate **312** having an aperture **314** may be disposed over substrate **500** such that ions impinge on substrate **500** through aperture **314**, which may be scanned with respect to substrate **500** along the y-direction. Referring also to FIG. **4**, the view of plate **312** shown in FIG. **4** is along the y-direction illustrated in FIG. **5***d*. FIG. **5***b* depicts a closer view of portion **502**, which includes patterned vertical resist lines **504**(long axes parallel to the y-direction), horizontally arranged lines **506** (long axes parallel to the x-direction), and blanket portion **508**. The substrate portion **502** is depicted after exposure of the resist features to an exemplary wide angular ion flux **530**, followed by exposure to a liquid etchant used for the purposes of mimicking a resist development process. Ion flux **530** is shown in the figures, although the structure of resist features shown in the figures corresponds to their resulting structure after ion bombardment is terminated followed by subsequent exposure to liquid etchant.

[0053] As illustrated in the figures, in this example, the ions **530** impinge upon the substrate portion **502** generally parallel to the y-direction (as defined in FIG. **4** and FIGS. **5**) and over a range of incidence angles, as illustrated further in FIG. **5***d*. In FIG. **5***d*, each resist line **506** is impacted by ions **530** on the top portion of the resist line and along sidewalls **518**. The results of etching the various resist features are shown in a top plan view in FIG. **5***b* and in cross-section along the lines A-A' and B-B' in FIGS. **5***c* and **5***d*, respectively. As evident, a preferential etching of portions of the resist features occurs, which illustrates the effect of the exemplary wide angular ion bombardment on the etch resistance of patterned resist features.

[0054] In particular, those portions of the resist features that are not subject to ion bombardment are highly susceptible to etching. For example, blanket region **508** has a horizontal edge **516**, which is exposed to ions **530** and a vertical edge **514**, which is disposed parallel to ions **530** and therefore does not receive direct ion bombardment from ions **530**. As shown in FIG. **5***b*, substantial resist etching occurs over a length L that extends inwardly from unprotected (that is, unbombarded) vertical edge **514**. Similarly, vertical lines **504**, which each have a pair of unprotected vertical edges **510**, are substantially etched across their individual widths W, which distance is less than etch length L. Accordingly, the entire width of the lines **504** is substantially attacked by etching. On the other hand, horizontal lines **506**, which are subject to ion bombardment along their entire sidewalls **518**, are substantially protected from etching, save for regions **540** immediately adjacent to small vertical notches **520**, which do not receive ion bombardment.

[0055] Accordingly, embodiments of the present invention may employ an exemplary plasma sheath modifier to subject patterned resist lines to a wide angular ion flux in order to harden the patterned resist features to subsequent processing. Such subsequent processing may include, for example, etchants that readily attack unhardened resist. In some embodiments, the patterned resist features may be arranged such that their sidewalls and tops are oriented to receive wide angular ion bombardment from an exemplary extraction plate.

[0056] In one embodiment of a double patterning lithography process, in a first step, a first set of patterned resist features (reliefs) is formed using a first lithographic process sequence. In a subsequent step, the first set of patterned resist features are subjected to a first exposure that comprises wide angular ion bombardment. The resist features may be arranged so as to expose both sidewalls and tops of the resist features to ion flux. In this manner, some or all resist surfaces that may be exposed to subsequent etchants may be hardened to resist the etchant attack. The wide angular ion bombardment may be carried out using a plasma sheath modifier arranged to simultaneously expose the sidewalls and tops of the resist features to ions. In a further step, a second lithographic process sequence is performed so as to define a second set of patterned resist features. In various embodiments, the first exposure hardens the first set of resist features in a manner that reduces or prevents the resist features from being degraded, such as being etched by chemical treatment or melted during the second lithographic processing sequence.

[0057] In various other embodiments, additional substrate relief features, such as permanent features that remain in the substrate after final processing, may be exposed to wide angular ion flux. In some embodiments, semiconductor substrate features may be ion implanted in a wide angular ion flux exposure using an extraction plate having a plasma sheath modifier. The semiconductor substrate features may be small semiconductor relief features, such as silicon-based materials including Si, SiGe alloys, or similar materials. This may be useful in the formation of devices that employ single crystal semiconductor features, such as in known FINFET double gate devices. For example, in some process sequences, a silicon structure, such as a channel region of a FINFET, may be subjected to an ion implantation process. In conventional ion implantation procedures, the external shape of such silicon fins may be substantially altered by ion implantation, which may adversely affect device performance by the eventual transistors formed using the FINFET process.

[0058] FIG. **6** depicts a profile of silicon relief features **602** after exposure to a conventional 1.4 kV Ar ion implantation process. In this example, the width of such features is on the order of 100 nm. As shown, the top portions **604** exhibit strong faceting and the sidewalls are generally sloped. In addition, the top of such features may be partially etched, reducing the overall height of such features.

[0059] In contrast, similar silicon relief features **702**, which are exposed to an exemplary wide angular Ar ion implantation process at 4 kV, show minimal faceting in top regions **704** and exhibit generally straight sidewalls, as depicted in FIG. **7**. Thus, the exemplary wide angular ion implantation may result in a more ideal structure for a device fabricated from silicon relief features **702**. This, in turn may facilitate better device performance.

[0060] Although the aforementioned embodiments of the invention are generally directed to systems and processes that employ ion bombardment for reducing roughness in surface features, as well as reducing the loss in critical dimension that may occur with such smoothening processes, other embodiments provide mechanisms that employ ion bombardment for adding material to surface patterned features. Referring to FIGS. **8***a* and **8***b*, there are shown a simplified illustration of

a technique for processing a 3D structure, according to another embodiment of the present disclosure. In this embodiment, a technique for decreasing the area of a hole is shown. In this embodiment, the substrate **800** may be a metallic substrate, a semiconducting substrate, or dielectric substrate. The substrate **800** may comprise a hole **812**. Although the present embodiment may be described in context to processing a substrate having a hole with first radius R_1, the present disclosure is not limited thereto. Similar to the photoresist of the earlier embodiment, the substrate **800** in the present embodiment may simply be a structure having one or more vertically extending surfaces.

[0061] In the present embodiment, ions **310** are directed toward the sidewall surface **814** of the hole **812** at multiple incident angles. As depicted, the sidewall **814** forms and angle with respect to the top surface **816** of substrate **800**, which may be about 90 degrees in some embodiments. Although ions are preferred, the present invention does not preclude other particles including radicals or other neutrals. The ions **310** directed toward the surface of the hole **812** may then be deposited onto the surface of the hole **812** thereby forming a boundary layer **822** having a second radius R_2. By using the plasma sheath modifier **822**, the ions **310** may be directed toward the surface of the hole **812** at multiple incident angles. As a result, a conformal, isotropic deposition may occur, and the boundary layer **822** with uniform thickness may form. Further, a radius of the original hole in the substrate **800** may decrease from R_1 to R_2, conformally and uniformly.

[0062] The methods described herein, may be automated by, for example, tangibly embodying a program of instructions upon a computer readable storage media capable of being read by machine capable of executing the instructions. A general purpose computer is one example of such a machine. A non-limiting exemplary list of appropriate storage media well known in the art includes such devices as a readable or writeable CD, flash memory chips (e.g., thumb drives), various magnetic storage media, and the like.

[0063] In summary, the present invention provides novel and inventive methods and systems for treating patterned features, such as photoresists or permanent substrate relief structures. The present invention can be deployed in systems that employ relatively low ion energy, such as plasma immersion systems, which affords the ability to provide ions and other species that have only a small penetration depth into the patterned features. This facilitates the ability to provide surface smoothening without substantially impacting resist pattern attributes, such as profile, and CD. By providing a substantial flux of ions at angles far from the normal, the PSM architecture of the present invention is especially effective in attacking resist features in areas most directly affected by surface roughness, that is, the resist sidewalls. Embodiments of the present invention, such as those employing inert gas plasmas, are not susceptible to pattern dependent effects that are prevalent using dry chemical processes, such as RIE. Furthermore, by employing a plasma sheath modulator in conjunction with plasma process systems, such as immersion implantation systems, the present invention offers a large flexibility for tailoring resist treatment processes. This is due to the variety of plasma parameters that can be conveniently and independently tuned, such as gas composition, ion energy, ion dose, and range of angles of incidence of ions.

[0064] The present invention is not to be limited in scope by the specific embodiments described herein. Indeed, other various embodiments of and modifications to the present disclosure, in addition to those described herein, will be apparent to those of ordinary skill in the art from the foregoing description and accompanying drawings. Although the present invention may be deployed in plasma immersion ion implantation systems using low energy ions, ion bombardment effects other than, or in addition to ion implantation, may contribute to resist smoothening, and the present invention may be deployed in other plasma systems capable of providing low energy ions.

[0065] Moreover, in addition to implanting or depositing, the techniques disclosed in the present disclosure may be used to perform etching on the photoresist structure or a structure other than the photoresist structure. For example, the techniques disclosed in the present disclosure may be used to perform photoresist trim process to reduce the critical dimension of the gate on a transistor. Contrary to the conventional trim process where the trim process is performed one surface at a time using by 0_2+HBr plasma, the technique of the present disclosure may be used to direct etching agents (e.g. ions) at multiple angles and perform the trim process isotropically on multiple surfaces at the same time. As such, the trim process may be performed much efficiently and more uniformly. Thus, such other embodiments and modifications are intended to fall within the scope of the present disclosure. Further, although the present disclosure has been described herein in the context of a particular implementation in a particular environment for a particular purpose, those of ordinary skill in the art will recognize that its usefulness is not limited thereto and that the present disclosure may be beneficially implemented in any number of environments for any number of purposes. Accordingly, the subject matter of the present disclosure should be construed in view of the full breadth and spirit of the present disclosure as described herein.

What is claimed is:

1. A method of treating resist features, comprising:

generating a plasma in a process chamber having a plasma sheath adjacent to a first surface of a substrate facing the plasma sheath; and

modifying a shape of a boundary defined between the plasma and the plasma sheath with a plasma sheath modifier wherein a portion of the shape of the boundary is not parallel to a plane defined by the first surface of the substrate wherein ions from the plasma impinge on the substrate surface over an angular range relative to the plane.

2. The method of claim **1**,

wherein the modifying operation comprises creating a gap defined by a pair of parts, the parts comprising one of insulators, semiconductors, and metals;

and wherein the shape of the boundary about the gap is a convex shape relative to the plane.

3. The method of claim **1**,

wherein the modifying operation comprises creating a gap within a plate, the plate comprising one of an insulator, conductor, and semiconductor;

and wherein the shape of the boundary about the gap is a convex shape relative to the plane.

4. The method of claim **2**, wherein the range of incident angles is between about positive 60° and negative 60° centered about 0.°

5. The method of claim **1**, wherein an energy and species of ions is arranged to substantially reduce a linewidth roughness of patterned resist features on the substrate.

6. The method of claim **1**, wherein the first exposure is sufficient to produce a substantial decrease in low frequency LWR.

7. The method of claim **1**, wherein the ions from the plasma are inert gas ions.

8. A method of patterning a substrate, comprising:

providing a first set of patterned resist features on the substrate;

exposing the first set of patterned resist features to a first exposure of ions extracted from a plasma sheath modifier operable to provide ions incident on the substrate over an angular range relative to the substrate; and

performing a lithographic patterning process on the substrate to form a second set of patterned resist features.

9. The method of claim **8**, wherein the first and second set of patterned resist features are formed using a double patterning lithographic process.

10. The method of claim **8**, wherein the first exposure is operable to harden the first set of patterned resist features which remain intact during the lithographic patterning process used to form the second set of patterned resist features.

11. The method of claim **8**, wherein the plasma sheath modifier comprises a first insulator portion and a second insulator portion that define a gap therebetween, such that a shape of a boundary of the plasma proximate the gap is a convex shape relative to a plane of the substrate.

12. The method of claim **8**, wherein the first exposure comprises an exposure to inert gas ions.

13. The method of claim **8**, wherein ion energy of the ions of the first exposure is less than about 20 keV.

14. The method of claim **8** wherein a linewidth roughness of the first set of patterned resist features is substantially reduced after the first exposure.

15. The method of claim **8**, further comprising exposing the first set and second set of patterned resist features to a second exposure of ions extracted from a plasma sheath modifier operable to provide ions incident on the substrate over a wide angular range, wherein a linewidth roughness of the second set of patterned resist features is reduced after the second exposure.

16. A method for implanting patterned crystalline features in a substrate, comprising:

generating a plasma in a plasma chamber having a plasma sheath adjacent to a first side of a substrate positioning the process chamber;

modifying a shape of a boundary between the plasma and the plasma sheath with a plasma sheath modifier so that a portion of the shape of the boundary is not parallel to a plane defined by a front surface of the substrate facing the plasma; and

providing a bias between the substrate and plasma, wherein ions implant into the patterned crystalline features over a wide range of angles without causing faceting in the patterned crystalline features.

17. The method of claim **16**, wherein the patterned crystalline features are silicon-based features.

18. A method of treating a hole in a substrate, comprising:

generating a plasma in a process chamber having a plasma sheath adjacent to a first surface of a substrate facing the plasma sheath, wherein the substrate comprises a hole sidewall surface that forms an angle with respect to the first surface; and

modifying a shape of a boundary defined between the plasma and the plasma sheath with a plasma sheath modifier wherein a portion of the shape of the boundary is not parallel to a surface defined by the first surface of the substrate wherein ions from the plasma impinge on the sidewall surface of the hole over an angular range.

19. The method of claim **18**, wherein the ions comprise species arranged to condense upon the surface of the hole.

20. The method of claim **18**, wherein the modifying operation comprises creating a gap within a plate, the plate comprising one of an insulator, metal, and semiconductor;

and wherein the shape of the boundary about the gap is a convex shape relative to a plane defined by the first surface of the substrate.

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